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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/635,638	08/07/2003	Akinobu Kawamura	Q76770	8799

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SUGHRUE MION, PLLC
2100 PENNSYLVANIA AVENUE, N.W.
SUITE 800
WASHINGTON, DC 20037

EXAMINER	
MAI, LAM T	

ART UNIT	PAPER NUMBER
2819	

DATE MAILED: 03/29/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/635,638	KAWAMURA, AKINOBU	
	Examiner	Art Unit	
	Brian Young	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 August 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-4 are rejected under 35 U.S.C. 102(e) as being anticipated by Fei et al.

3. Claim 1 recites "a variable-order delta sigma modulator comprising means that vary a combination of plural integrators constituting a delta sigma modulator to thereby vary an order of the delta sigma modulator, wherein the means vary the order of the delta sigma modulator into an optimum order in relation to a sampling frequency.

4. Fei et al disclose a "***Variable Order Modulator***" (title). Their abstract recites "a ***delta-sigma modulator 400 includes circuitry 407 for selectively varying an order of the modulator to vary a modulation index of the delta sigma modulator".***

5. The specification describes figure 4 as follows "FIG. 4 is a functional block diagram of the first three stages of an nth order feedforward delta-sigma modulator 400. It should be noted that the order may change from specific design to specific design, depending on such factors as the required noise shaping response and stability concerns. Moreover, while a feedforward design operating on a digital input is shown, other designs can be used, including those operating on an analog input stream. The input stream is received at the non-inverting input of input summer 401 and summed with feedback received from the quantizer at the summer inverting input. For an nth

order modulator, the filter comprises n number of integrator stages 402, the outputs of which are summed by output summer 405. In the illustrated embodiment, the output of at least some integrator stages 402 is feedback to a inverting summer 403 of the previous stage through a gain stage 404. The summed output from summer 405 is then requantized by quantizer 406 and passed to DAC 203 and eventually the output amplifiers. ***In order to vary the order of the modulator, a set of multiplexers (selectors) 407 are provided between integration stages***. To decrease the order of the modulator, selected integrator stages 402 are removed, preferrably starting with the last currently active stage in the chain, by switching the input of the selected stage or stages from the output previous integrator stage to a logic zero (or 0 volts in the case of an analog modulator). The contribution of the removed stages or stages at the summer 405 is effectively zero. To increase the modulator order, active stage are returned to the chain, preferrably beginning with the last currently active stage, by switching the corresponding input of the selected stages back to the output of the previous stage.

6. The modular disclosed by Fei et al. is also implemented in a DAC "***FIG. 2 is a functional block diagram of one channel of a DAC 200 according to the principles of the present invention and suitable for use in DAC subsystem 100***. DAC 200 includes a gain stage (multiplier) 201 and Delta-Sigma modulator 202, which re-codes and quantizes the output from multiplier 201. The m-level data output from modulator 201 is passed through a switched-capacitor, or other conventional multiple-bit DAC circuit 203, and converted into the analog domain. Analog low pass filter 204 then filters the analog signal. Dynamic element matching (DEM) logic 205 may be provided for

shaping noise which may result from DAC element mismatch. Multiplexer 207 selects between traditional multi-bit PCM data and single-bit data at the modulator input.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brian Young whose telephone number is 571-272-1816. The examiner can normally be reached on Mon-Fri 7:30-4:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mike Tokar can be reached on 571-272-1812. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Brian Young
Primary Examiner
Art Unit 2819

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